

<b>Notice of References Cited</b>	Application/Control No. 10/071,262	Applicant(s)/Patent Under Reexamination BRYANT ET AL.	
	Examiner Cynthia Britt	Art Unit 2133	Page 1 of 1

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	B	US-5,572,712	11-1996	Jamal, Kamran	716/18
	C	US-6,463,560	10-2002	Bhawmik et al.	714/733
	D	US-5,878,051	03-1999	Sharma et al.	714/724
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#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Methods for Boundary Scan Access of Built-in Self-test for Field Programmable Gate Arrays" Hamilton et al. IEEE Southeastcon '99 Proceedings 25-28 March 1999 pages 210 - 216 Inspec Accession Number: 6422210
	V	"Iterative Improvement Based Multi-way Netlist Partitioning for FPGAs" Krupnova et al. This paper appears in: Design, Automation and Test in Europe Conference and Exhibition Proceedings 9-12 March 1999 pages 587 - 594 Inspec Accession Number: 6390095
	W	"Layout-Driven High Level Synthesis for FPGA Based Architectures" Xu et al. Design, Automation and Test in Europe Proceedings 23-26 Feb. 1998 pages 446 - 450 Inspec Accession Number: 5906838
	X	"Boundary Scan Access of Built-in Self-test for Field Programmable Gate Arrays" Gibson et al. IEEE International ASIC Conference and Exhibit, Date: 7-10 Sept. 1997 pages 57-61 Inspec Accession Number: 5774208

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.